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AUG 24 2006

REMARKS

Claims 1-4 are pending in the application. Claim 1 has been amended by the present amendment to specifically recite the order of steps. The amendment is fully supported by the application as originally filed.

Applicants' claimed invention is directed to a method for fabricating a thermally-enhanced wafer-level chip scale package, including the steps of:

(1) preparing a semiconductor wafer predefined into a plurality of integrated circuit chips, then proceeding to step (2);

(2) performing a bumping process, then proceeding to step (3);

(3) performing a back-side lapping process to grind away a back-side portion of the semiconductor wafer, then proceeding to step (4);

(4) attaching a thermally-conductive stiffener to the back side of the semiconductor wafer, then proceeding to step (5);

(5) performing a singulation process to cut the thermally-conductive stiffener and cut apart each chip from the semiconductor wafer, then proceeding to step (6);

(6) performing a flip-chip die bonding process.

For example, the bumping process is performed prior to the back-side lapping/grinding process for the wafer. As amended, claim 1 requires that steps (1) to (6) must be performed in the order recited in the claim.

Claims 1 and 3 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 6,392,290 to Kasem et al. ("Kasem"). Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Kasem in view of U.S. Patent 6,403,882 to Chen et al. ("Chen"). Claim 4 was rejected under 35 USC 103(a) as being unpatentable over Kasem in view of U.S. Patent 6,550,531 to Scarls et al. These rejections are respectfully traversed.

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Kasem does not teach or suggest a fabrication method in which a bumping process is performed prior to a back-side lapping/grinding process.

In Kasem, a method for fabricating a package includes steps performed in the following order. First, a chip 220 is prepared (see column 9, line 24 to column 10, line 13; and FIGS. 47A-53C). Then, a semiconductor substrate 227 of the chip 220 is thinned by grinding its back side (see column 10, lines 14-21; and FIGS. 54A-54C). Then, a heat sink 245 is bonded to the back side of the thinned substrate 227 using an adhesive layer 246 (see column 10, lines 23-26; and FIGS. 55A-55C). Then, solder bumps 248 are formed over a front side of the chip 220 (see column 10, lines 30-34; and FIGS. 56A-56C). Then, the substrate 227 is sawed at locations 250 "to separate it from the portions of the substrate in other chips on the wafer. The heat sink 245 is left intact" (column 10, lines 35-38 (emphasis added); FIGS. 57A-57C). Finally, the chip 220 is separated from other chips in the wafer by sawing through the heat sink 245 at locations 252 (see column 10, lines 40-42; and FIGS. 58A-58C).

In the method of Kasem, as described above, the step of forming solder bumps 248 occurs after a step of lapping/grinding the substrate 227. In contrast, the Applicants' claimed invention requires a bumping process to be performed prior to a back-side lapping process.

On page 6 of the Office Action of 02/24/2006, in the "Response to Arguments" section, it was indicated that claim 1, as previously worded, did not recite that step (2) must be performed prior to step (3). However, as amended, claim 1 clearly requires that step (1) is performed, then step (2) is performed, and so forth, in the order stated in the claim.

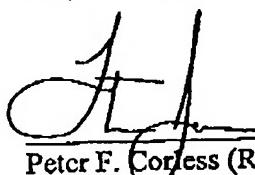
In other words, as amended, claim 1 requires "performing a bumping process..." in step (2), and then proceeding to step (3), which recites "performing a back-side lapping process..." The above sequence of steps is not taught or suggested by Kasem.

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For at least the reasons discussed above, the Kasem reference does not anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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